Amendments of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (CURRENTLY AMENDED) A method of operating a data processing device (100)~~, notably a chip card,~~ which includes an integrated circuit (10) which carries out, in dependence on a clock signal, arithmetic operations~~, notably~~for cryptographic operations, data input and data output (38) as well as data transfer (40) from and to registers of the integrated circuit (10),
characterized in that
the integrated circuit (10) is controlled in such a manner that the execution of actual arithmetic operations on the one hand and ~~the~~dummy data input/output operations (38) ~~as well as the~~or dummy data transfers (40) from one register to another or between registers (30, 32) on the other hand ~~is~~are executed in parallel in time.

2. (CURRENTLY AMENDED) A method as claimed in Claim 1,
characterized in that
~~directly before,~~ during ~~and/or directly after the~~ actual data transfer from one register to another or between the registers (30, 32) of the integrated circuit, a processor (28) of the integrated circuit (10) executes dummy calculations which act on random or predetermined data, no data being written into registers (30, 32) of the integrated circuit.

3. (CURRENTLY AMENDED) A data processing device (100)~~, notably a chip card,~~ which ~~is specifically intended to carry out a method as claimed in at least one of the preceding Claims, and~~ includes an integrated circuit (10) which executes arithmetic operations~~, notably~~for cryptographic operations, in dependence on a clock signal (20), the integrated circuit (10) including a processor (28) with an associated first register (30) and data inputs and outputs (24, 26),
characterized in that

a second register (32) is connected to the first register (30) and is provided with the data inputs and outputs (24, 26), a control unit (16) being connected to the integrated circuit (10) and being constructed in such a manner that during actual arithmetic operations for the cryptographic operations, it controls parallel operation in time of the registers (30, 32) for dummy data input/output (38) ~~and~~ or dummy data transfer (40) from register to register or between the registers (30, 32) on the one hand and the actual arithmetic operations (40) of the processor (28) on the other hand.

4. (ORIGINAL) A data processing device (100) as claimed in Claim 3, characterized in that the first register (30) is an operand register of the processor (28) and/or the second register (32) is an operand register for the data input/output (38).